SoC Design Verification and Validation Challenges

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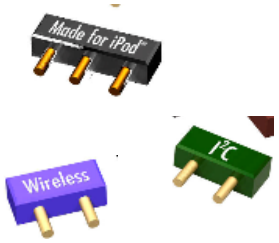
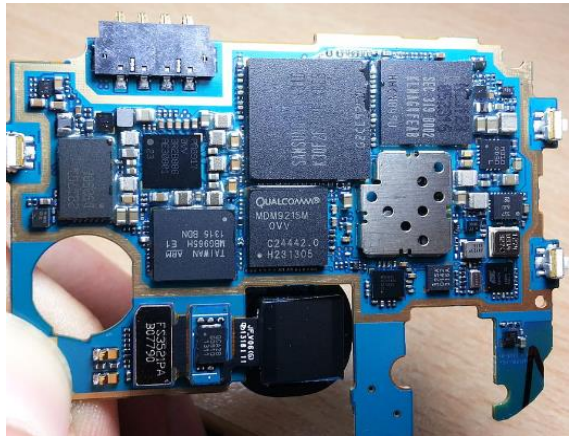
Agenda

- Overview of SoC
- Design Challenges
- Customer needs
- Solution

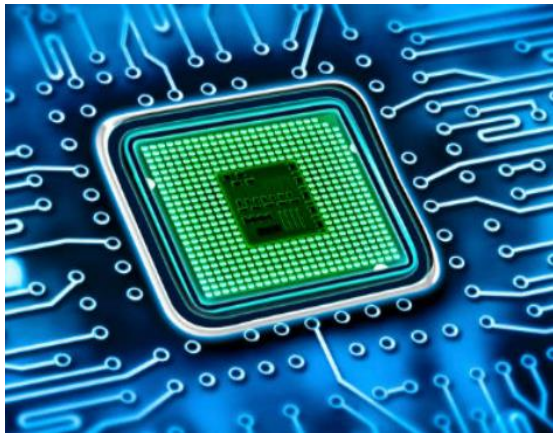
Introduction to SoC



chips



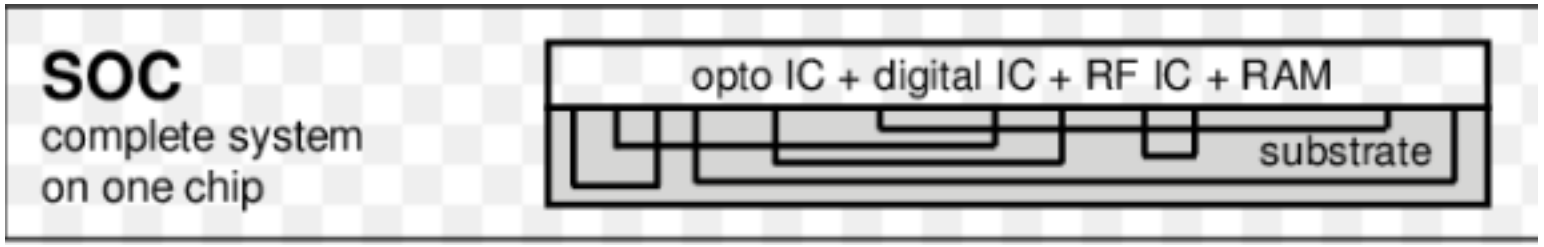
Circuit board



SoC

SoC is a Complex IC which has all major functions within a Chip or Chip set

- Programmable Processor
- On Chip Memory
- Analog Components
- Micro electronic opto & mechanical system
- Hardware and software



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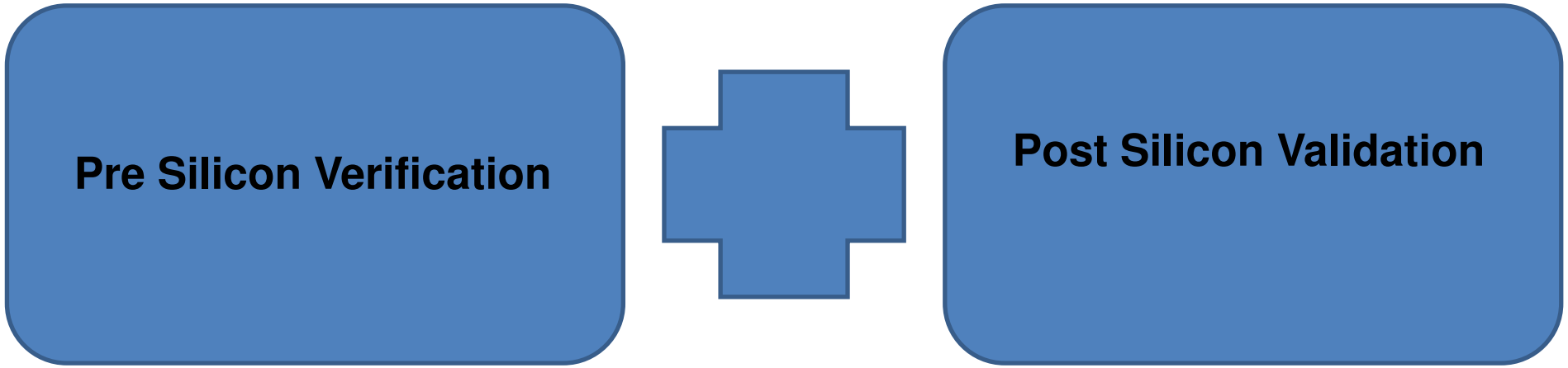
SoC Challenges

- Integration of more functions.
- Reduced Product Design Cycles
- Compressed verification and Validation Cycles.
- Time to market pressures
- Increasing device complexity (typically 30+ million logic gate)

SoC Challenges and Needs

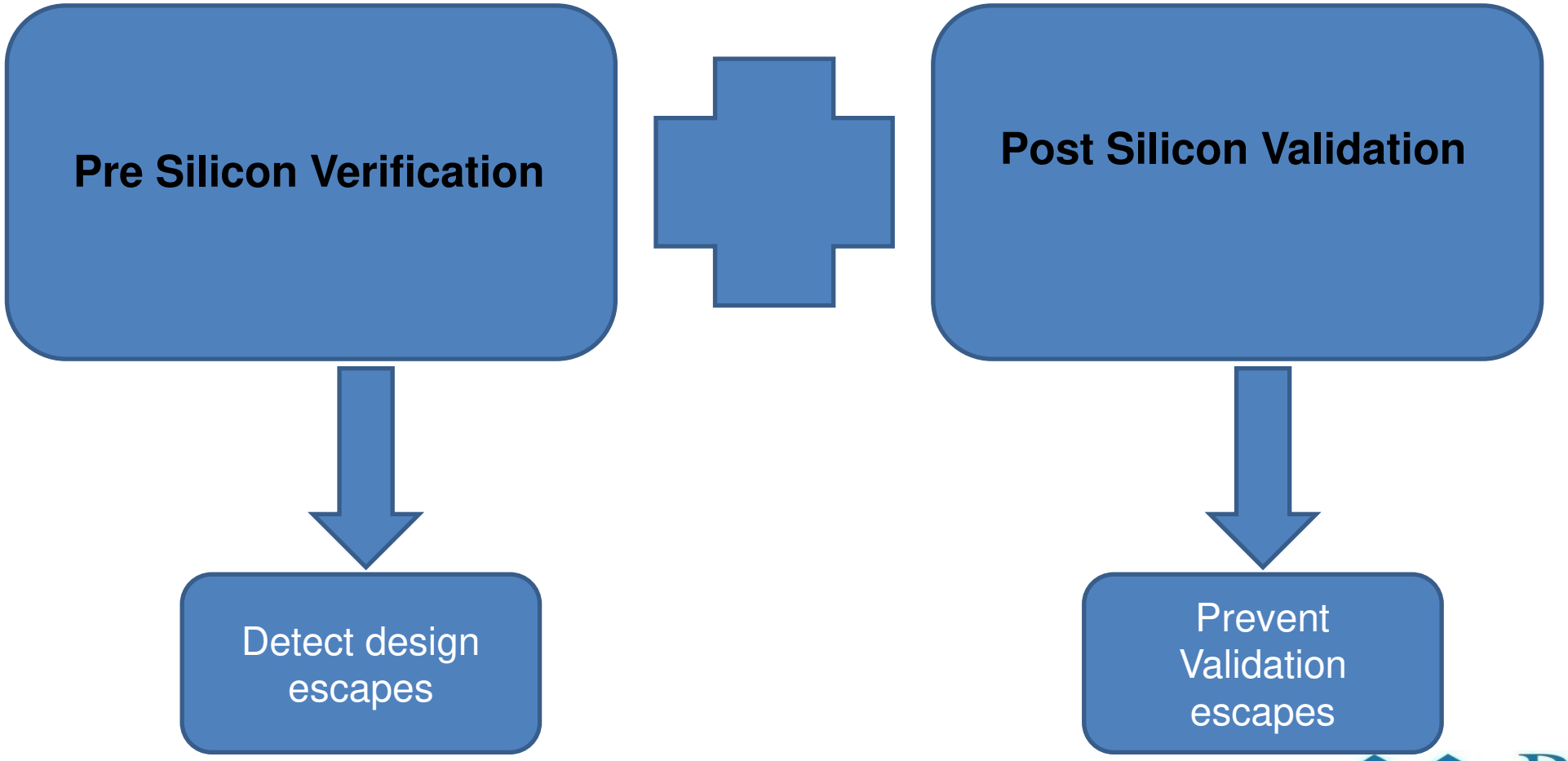


Ensures functional and Operational Quality of final product.

A single problem in any one functionality of the SoC can lead to re-spin leading to cost escalation and delays which may cost the market acceptance.

SoC Challenges and Needs

Ensures functional and Operational Quality of final product.



SoC Design and Verification Challenges

Design escapes

Functional errors which go un-noticed during design cycle:

- Incorrect functional requirements
- Wrong assumptions during design
- Defects in design.

Validation escapes

Defects in Silicon which go un-noticed during validation cycle:

- Complex data path/flow
- Multiple conditions
- Time pressure

Thumb rule: If you don't test it will not work!!!

SoC Design and Verification failure points

Pre Silicon Functional Verification

- Time consuming
- Urgency in Design to Silicon turn

Post Silicon Validation

- Test at Full performance
- Signal Integrity
- Issues with communicating with other peripherals
- Timing issues

Inter Operability

- Implementation Differences
- Custom Implementation
- Compatibility issues with different sources

SoC Design and Verification KEY points

- Early verification.
- Time to market pressures balanced with right set of test plans.
- Edge case Coverage in test cases
  - Cycle to Cycle tests
  - Transaction driven tests
  - Full performance tests
- Expert Validation Engineer needed to take decisions which can avoid delays.
- Detailed design verification is a MUST.
- Open communication across teams.
- Ensure logical and algorithmic correctness of each design block.
- System Validation tests, Compatibility validation tests . **C-M-V or "4 Corner" tests ,**Signal Integrity Validation tests , Manufacturing Validation tests and Performance Validation - **A MUST**

SoC – System Validation

System Validation tests:

- Isolates approximately 75% of defects**.**
- Typically is a specially designed validation board with probe points for
    1. Logic Analysers
    2. Access to bus signals
    3. Variable clock and voltage regulators
    4. JTAG debugging port.
    5. I/O ports
- Functional test ensures RTL logic accuracy.
- Compatibility Validation tests ensures near real application scenario is tested.

Defects found in this cycle are easy to fix.

“C-M-V” or “4 corner” testing

C-M-V stands for Circuit marginality Validation test also known as 4 corner test.

- C M V design is tested for :
  - Voltage sensitiveness
  - Temperature sensitiveness
  - Frequency sensitiveness
- **“4 corner test” tests a device at:**
  - High Voltage
  - Low Voltage
  - High Temperature
  - Low Temperature

Analyses failure ay 1 or more corners

Signal Integrity Validation testing

Signal-integrity validation tests:

- Critical in SOC devices that operate at high clock frequencies.

- Tests tight margins as it checks
  - electrical signals
  - Waveforms and
  - signal-integrity measurements as well as the quality of multiple interfaces.

- Identify problems with the electrical signals reaching their destination.
- Determine whether the signals have sufficient margins to interface with external chip sets, adapters, and other devices.
- Measures:
  - crosstalk
  - delay
  - glitch
  - Voltage drop, and
  - other electrical characteristics.

Manufacturing Validation testing

Manufacturing validation tests:

- Checks if we can manufacture a product in high volume without affecting yield.

- Tests if manufacturing-process variations do not impact product specifications and margins.

- Quality and reliability validation checks if the product has :
  - low infant-mortality rate and
  - low FIT (failure in time).

One can derive MTBF (mean time between failures) and FIT numbers from quality and reliability validation.

Performance Validation testing

Performance validation tests:

- Allows one to compares theoretical performance with the actual performance of the DUT.
- Benchmarking test suites checks the performance and generate metrics that provide the basis for any deviations between expected and observed results.
    - When testing reveals significant deviations, the design team can confirm the observations in simulations.
- May result in design-level changes that involve firmware or software workarounds or in a device re-spin.

Potential Solution

- RTL simulation tools
- Oscilloscopes
- Logic Analyzers
- Protocol Analyzers with Emulation , margin test and error injection capabilities.

Timing Analysis

Logic Analysis

Protocol Analysis

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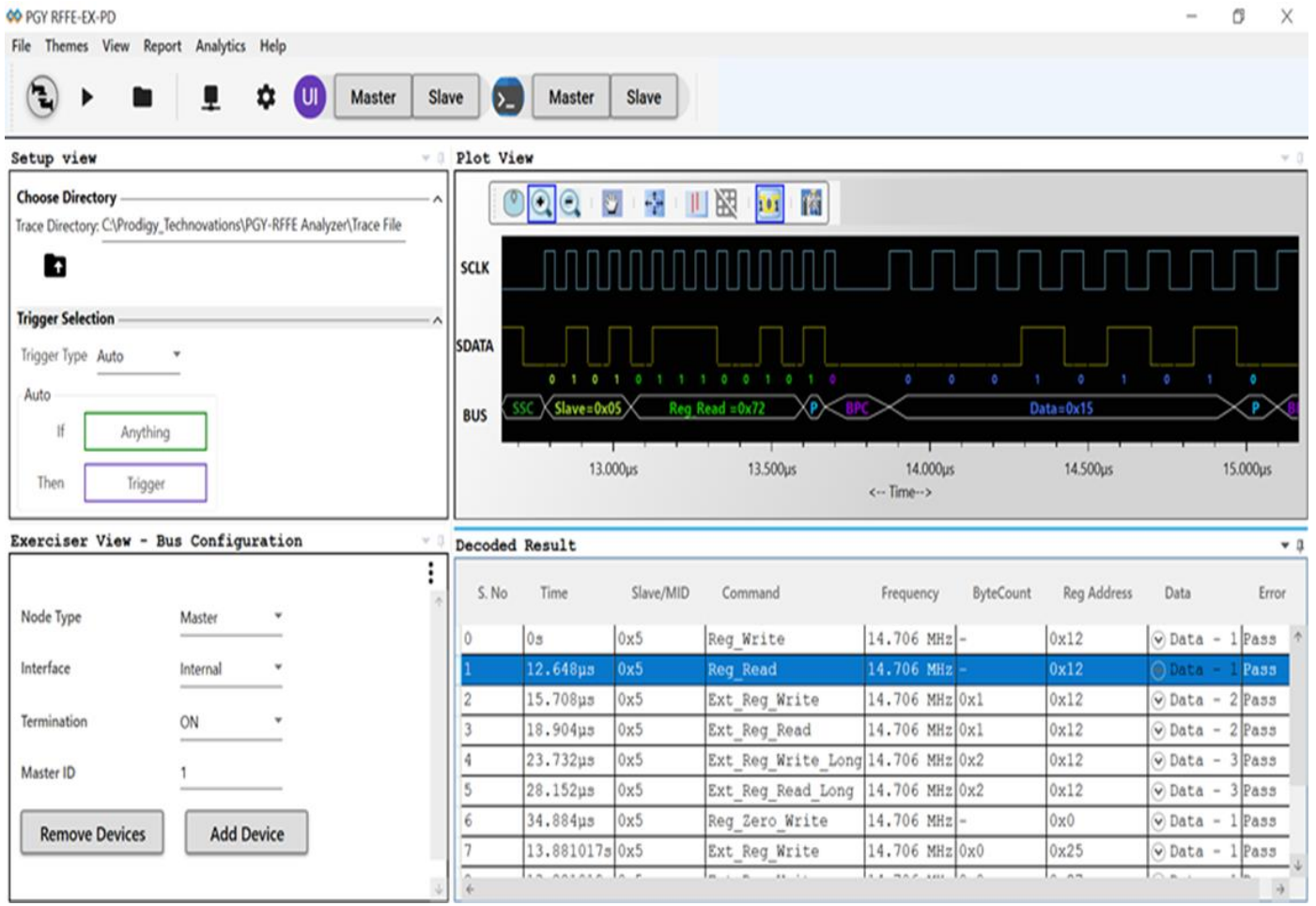
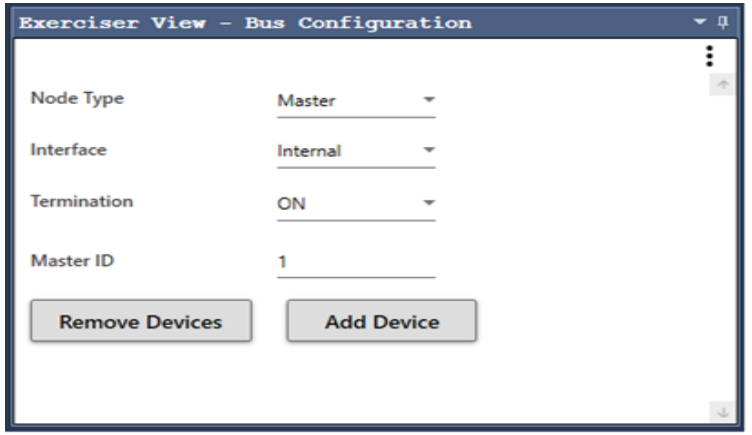
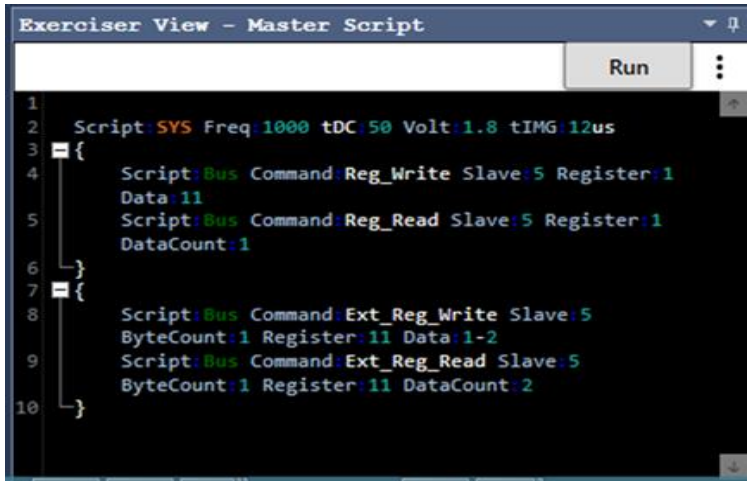
Capability of Test Solutions - 1

- Protocol Analyzers with Emulation , margin test and error injection capabilities.



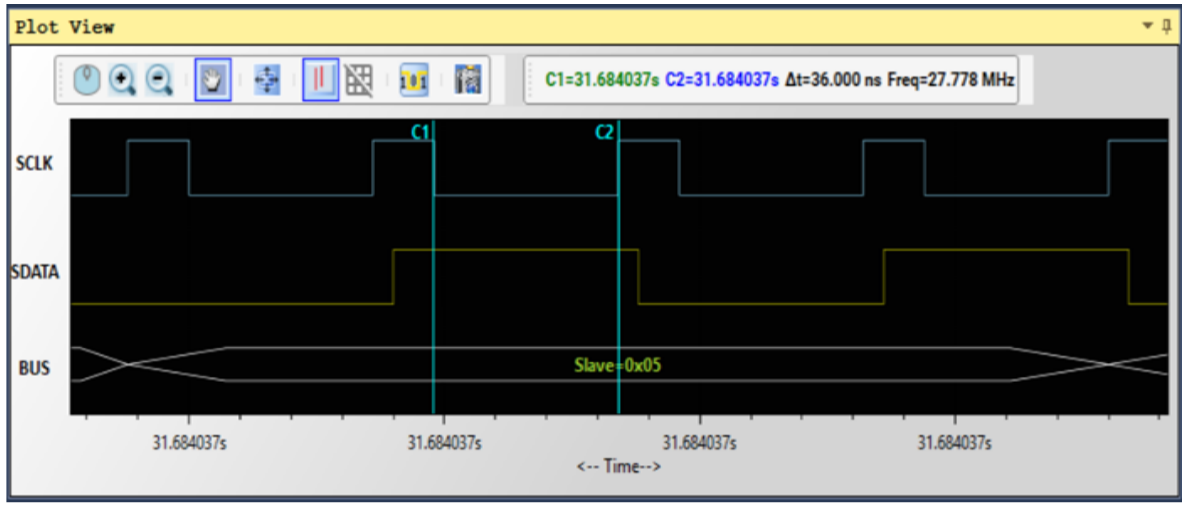


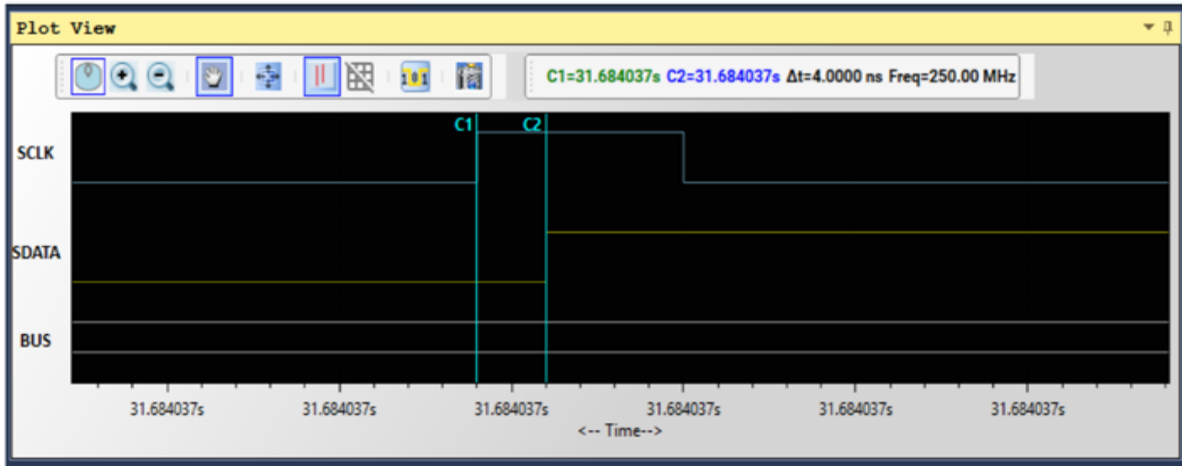


Capability of Test Solutions - 2

- Protocol Analyzers with Emulation , margin test and error injection capabilities.

  - Variable frequency
  - Generates standard amplitude signals
    - 1.0V to 3.3V
    - Worst case signal 0.6V to 3.6V
  - Timing
    - Ability to control Clk-Data delay
    - Ability to control duty cycle
  - API
    - Scripting capability in Phyton/C++ to enable
      - C-M-V or 4 Corner tests
      - SI Validation tests
      - Margin tests





Capability of Test Solutions - 3

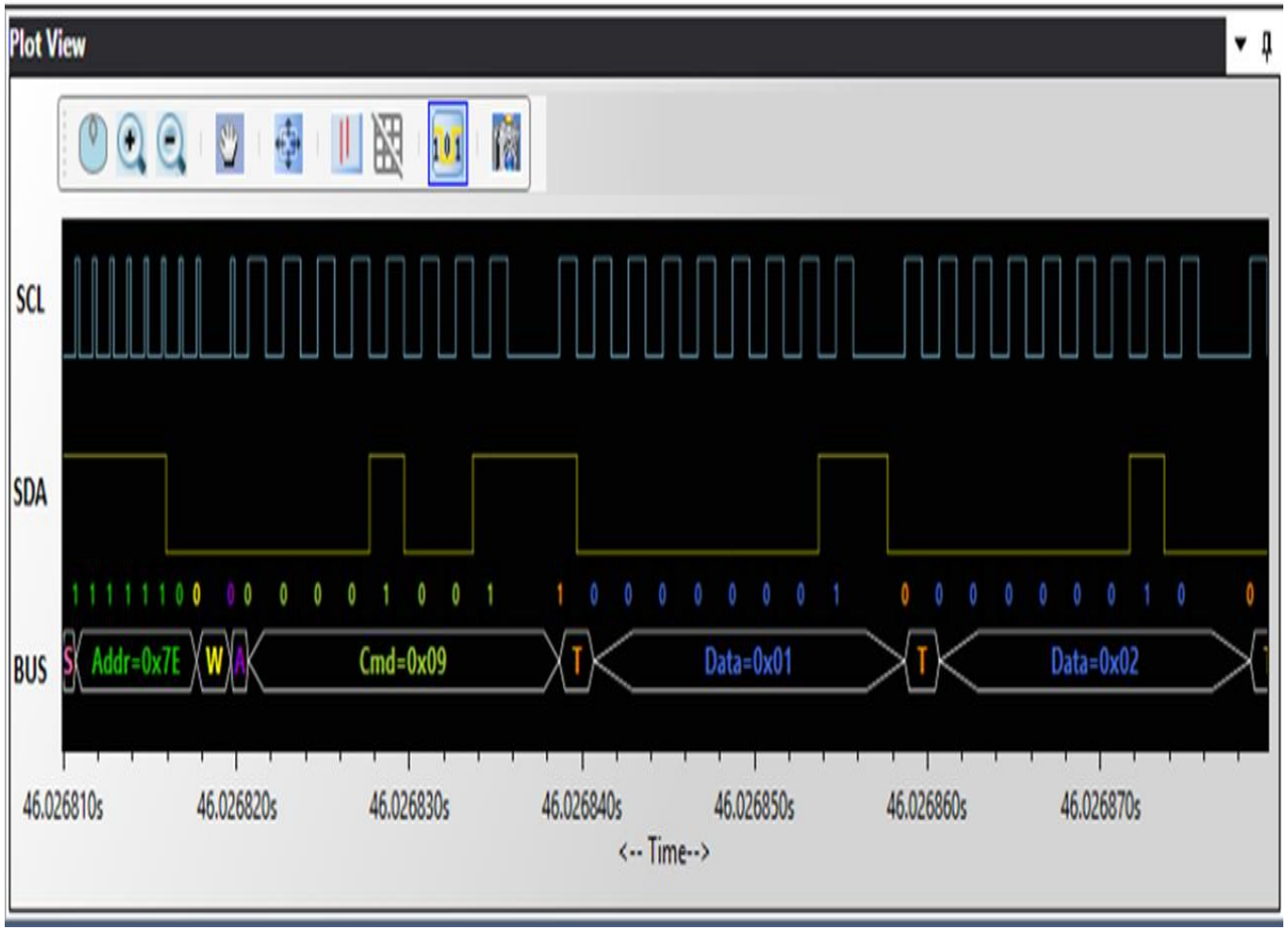
- Debug test tools

- Oscilloscopes
  - Specific Electrical and decode SW capabilities.

- Logic Analyser
  - State View
  - Timing View

- Protocol Analyser
  - Decode Bits stream

- API
  - Scripting capability in Phyton/C++ to enable
    - C-M-V or 4 Corner tests
    - SI Validation tests
    - Margin tests



Summary

- SOC design verification and Validation needs to be handled effectively to ensure:
  - Design issues are checked early
  - Silicon bugs are caught without fail.

  Else re-spins will be costly and time consuming.

- Needs rigorous test environment to cover
  - C-M-V or 4 corner testing
  - SI validation testing
  - Manufacturing Validation testing
  - Performance Validation testing

- Contact Prodigy Technovations for detailed solution information.

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